California State University, Northridge

Department of Electrical & Computer Engineering



ECE 526L

Lab 10 Report

By

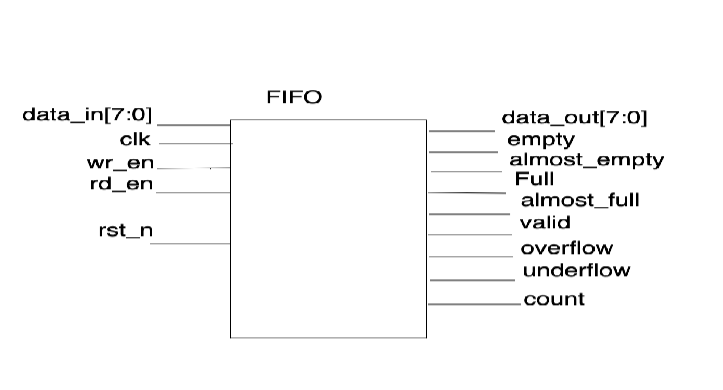
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**1: Introduction**

The objective of this lab a parameterized synchronous FIFO .

Here we have to use following diagram to build FIFO.



**2: Procedure**

**a. Part 1: Creating FIFO Module**

In this lab I have created a FIFO module. Inside the module I have assigned “CLK, reset, wr\_enable,wr\_data and rd\_enable ” as input variables and “empty and full” as output variable and CF, OF, SF, ZF,rd\_data, count as an output variables. Then I wrote the FIFO. After completing the code I ended the module using and saved the file with name “FIFO.v”.

**b. Part 4: Creating FIFO\_tb Testbench**

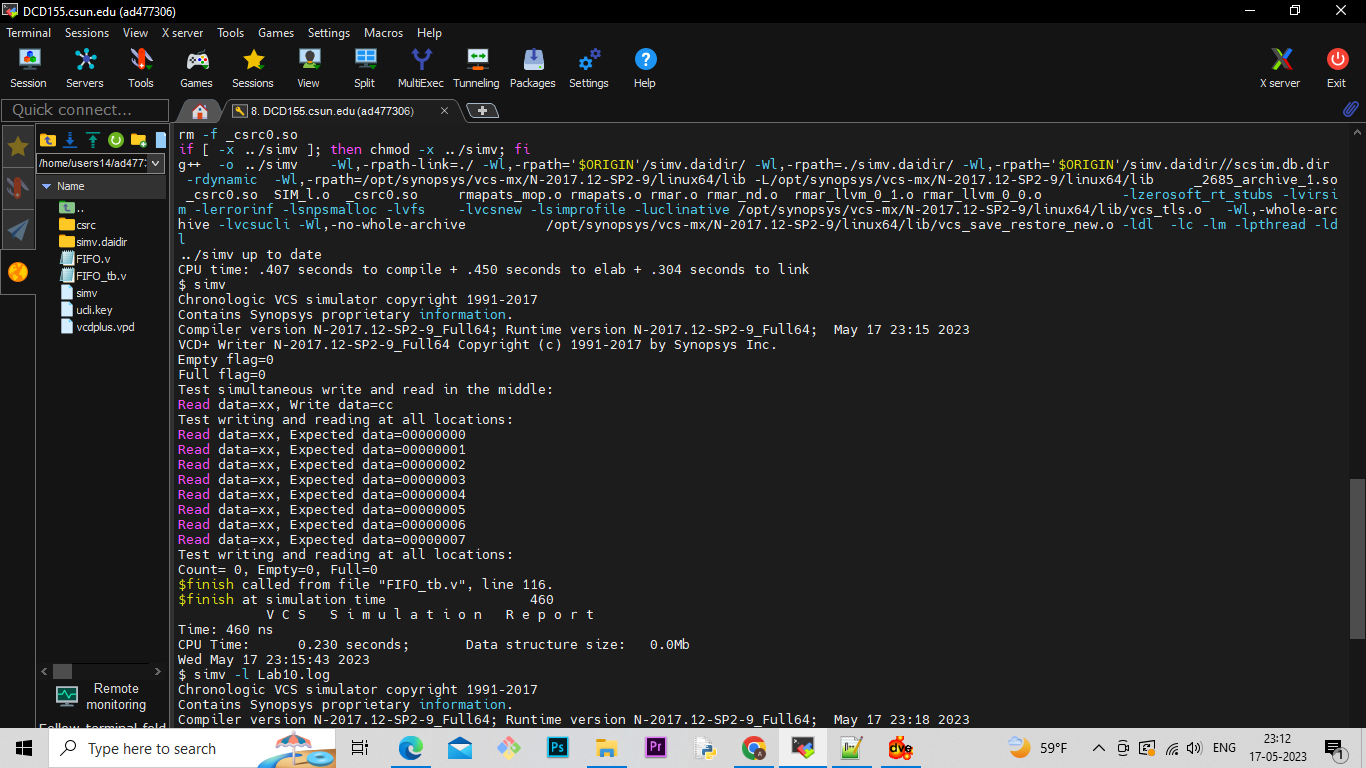
I have written the test bench for the **FIFO** module. We require test bench just to make sure that the module we have created is working properly.

**c. Part 3: execution.**

Using “vcs -debug -full64 FIFO.v FIFO\_tb.v” command I executed testbench file.

**d. Part 4: Simulation**

After an execution of all modules, I have run the command “simv” for simulation.

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**e. Part 5: Creating Log File**

After running the simulation I created the log file for first stategy using the “simv -l Lab8\_non\_exh.log” command

Command: /home/users14/ad477306/Verilog/Lab10/./simv -l Lab10.log

Chronologic VCS simulator copyright 1991-2017

Contains Synopsys proprietary information.

Compiler version N-2017.12-SP2-9\_Full64; Runtime version N-2017.12-SP2-9\_Full64; May 17 23:18 2023

VCD+ Writer N-2017.12-SP2-9\_Full64 Copyright (c) 1991-2017 by Synopsys Inc.

Empty flag=0

Full flag=0

Test simultaneous write and read in the middle:

Read data=xx, Write data=cc

Test writing and reading at all locations:

Read data=xx, Expected data=00000000

Read data=xx, Expected data=00000001

Read data=xx, Expected data=00000002

Read data=xx, Expected data=00000003

Read data=xx, Expected data=00000004

Read data=xx, Expected data=00000005

Read data=xx, Expected data=00000006

Read data=xx, Expected data=00000007

Test writing and reading at all locations:

Count= 0, Empty=0, Full=0

$finish called from file "FIFO\_tb.v", line 116.

$finish at simulation time 460

V C S S i m u l a t i o n R e p o r t

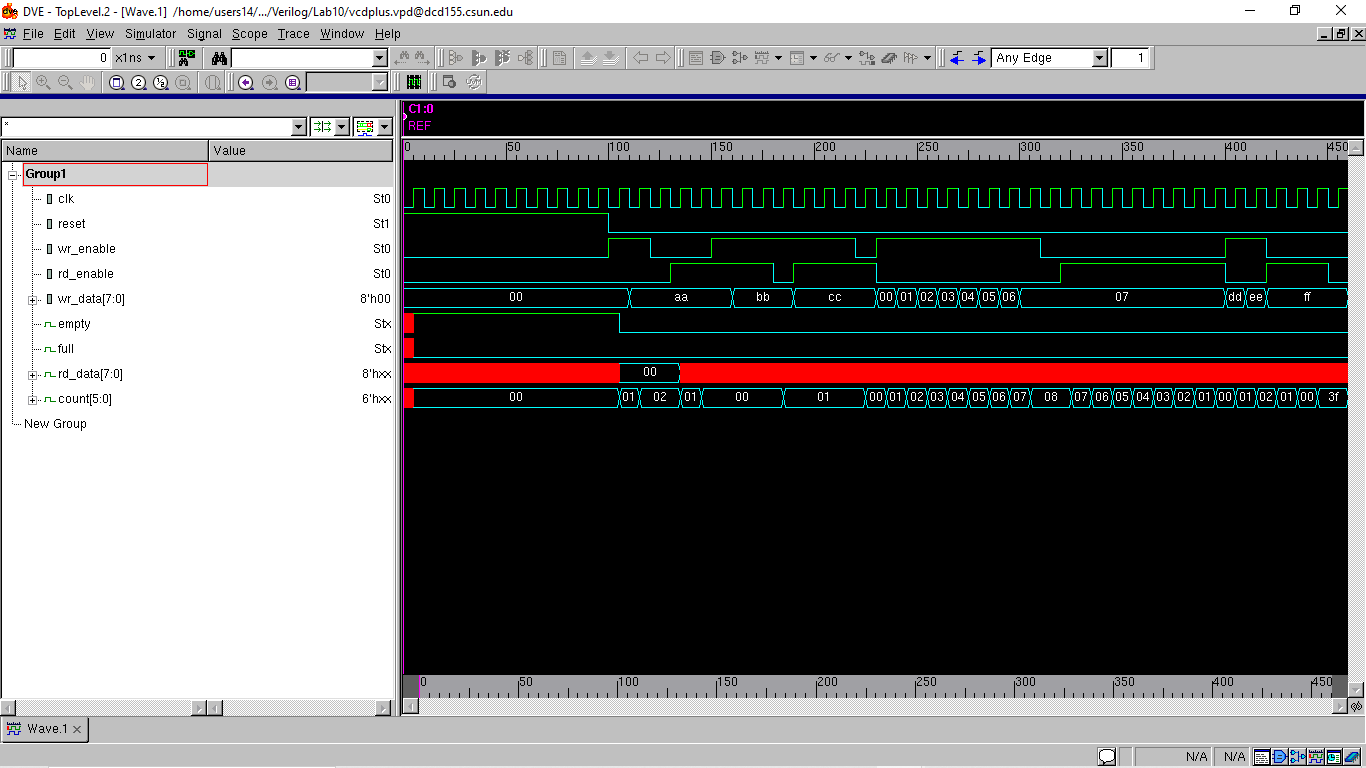
Time: 460 ns

CPU Time: 0.230 seconds; Data structure size: 0.0Mb

Wed May 17 23:18:09 2023

**f. Part 6: Seeing the waveform.**

After creating the log file I opened the DVE using “dve -full64 &” command to see the waveforms.

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**Conclusion:**

The constructed ALU unit in this experiment was verified of its functionalities. Using testbench I have successfully tested the FIFo functionality.

**Extra Credit:**

To modify the FIFO module to be asynchronous, you can remove the clock (clk) signal and the posedge clk sensitivity in the always blocks. Additionally, you can change the reset behavior to be asynchronous.

I hereby attest that this lab report is entirely my own work. I have not copied either code or text from anyone, nor have I allowed or will I allow anyone to copy my work.

Name (printed) Avinash Damse

Name(signed) Date : 14-May-2023

